LM16155
Dot Matrix LCD Unit

FEATURES

- Low Power Consumption
- Thin, Lightweight Design Permits Easy Installation in a Variety of Equipment
- General-Purpose CMOS:
  - The Unit can be Easily Interfaced to a Microcomputer with Common 4-Bit and 8-Bit Parallel Inputs and Outputs
- Built-in Character Generator ROM, RAM, and Display Data RAM:
  - Character Generator ROM – 160 Different 5 × 7 Dot Matrix Character Patterns
  - Character Generator RAM – Eight Different User-Programmed 5 × 7 Dot Matrix Patterns (Write Capability by Program)
  - Display Data RAM – 80 × 8 Bits
- Extensive Instruction Set:
  - Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Character Blink, Cursor Shift, and Display Shift
- Internal Automatic Reset Circuit at Power-On (Refer to the separate users manual for the operating conditions)
- Operates From a Single 5 V Power Supply and Incorporates an LCD Panel Which Provides a Highly Stable Display Over a Wide Range of Temperature

DESCRIPTION

The SHARP LM16155 Dot Matrix LCD Unit consists of a combination of a 5 × 7 dot 16-character 1-line dot matrix LCD panel, LCD driver, and controller LSI mounted on a single printed circuit board. Incorporating mask ROM-based character generator and display data RAM in the controller LSI, the unit is capable of efficiently displaying the desired characters under microcomputer control.

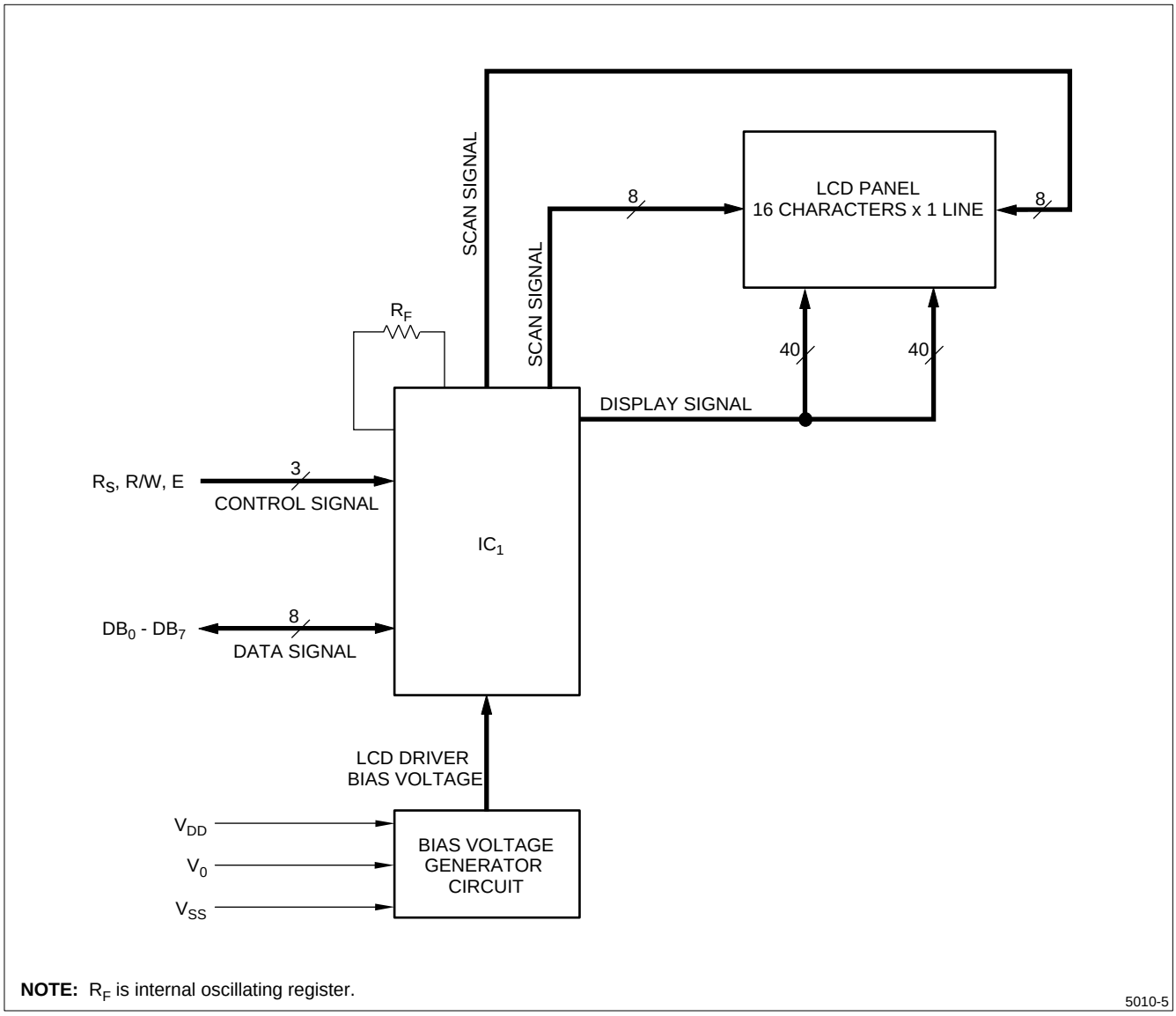


Figure 1. LM16155 Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT
Outline Dimensions	80 (W) × 36 (H) × 11 max (D)	mm
Active Area	64.5 (W) × 13.8 (H)	mm
Display Format	16 characters × 1 line	–
Character Format	5 × 7 dots, with cusor	–
Character Size	3.07 (W) × 5.73 (H) (5 × 7 dots)	mm
Dot Size	0.55 (W) × 0.75 (H)	mm
Dot Spacing	0.08	mm
Character Color	Dark blue	–
Backlight Color	White	–
Weight	Approximately 25	g

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD} - V_{SS}	Supply Voltage	–0.3	7.0	V
V_{IN}	Input Voltage	–0.3	V_{DD} +0.3	V
Tstg	Storage Temperature	–25	+70	°C
Topr	Operating Temperature	0	+50	°C
V_{DD} - V_O	Supply Voltage (LCD Drive)	0	13.5	V

ELECTRICAL CHARACTERISTICS (t_A = 25°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTES
$V_{DD} - V_{SS}$	Supply Voltage (Logic)		4.75	5.0	5.25	V	–
$V_O - V_{SS}$	Supply Voltage (LCD Drive)		–	1.0	–	V	V_{DD} = 5.0 V
V_{IL}	Input Voltage	'L'	–0.3	–	0.6	V	–
V_{IH}		'H'	2.2	–	V_{DD}	V	–
V_{OL}	Output Voltage	'L'	–	–	0.4	V	I_{OL} = 1.2 mA
V_{OH}		'H'	2.4	–	–	V	I_{OH} = –0.205 mA
I_{IL}	Input Leakage Current		–	–	1	µA	–
f_{OSC}	Internal Oscillating Frequency		–	250	–	kHz	–
I_{DD}	Supply Current (Logic)		–	1.5	2	mA	V_{DD} = 5 V V_O = 0 V
P_D	Power Dissipation		–	7.5	10	mW	

INTERFACE TIMING (V_{DD} = 5.0 V ±5%, t_A = 0 to 50°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{CYCE}	Enable Cycle Time	1000	–	–	ns
PW_{EH}	Enable Pulse Width	450	–	–	ns
t_{ER}, t_{EF}	Enable Rise/Fall Time	–	–	25	ns
t_{AS}	RS, R/W Setup Time	140	–	–	ns
t_{AH}	Address Hold Time	10	–	–	ns
t_{DSW}	Data Setup Time	195	–	–	ns
t_{DDR}	Data Delay Time	–	–	320	ns
t_H	Data Hold Time (Write)	10	–	–	ns
t_{DHR}	Data Hold Time (Read)	20	–	–	ns

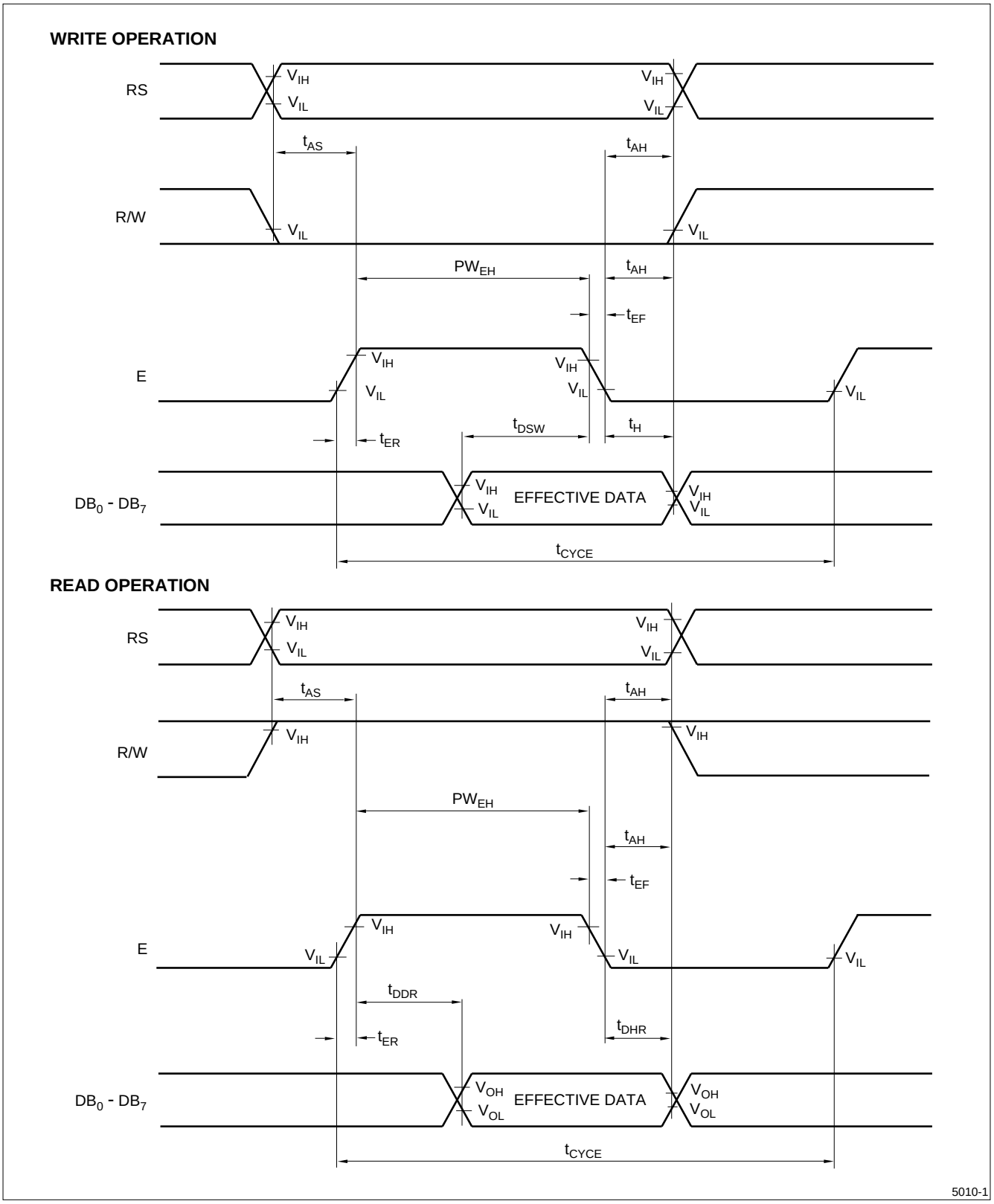


Figure 2. Interface Timing Chart

PIN CONNECTIONS

PIN NUMBER	SYMBOL	DESCRIPTION	CONNECTION
1	V_{SS}	Ground Potential	GND: 0 V
2	V_{DD}	Power Supply (Logic)	+5 V Power Supply
3	V_O	Contrast Adjustment Voltage	Adjust the contrast by supplying voltage from 0 V to 5 V
4	RS	Register Select Pin	Control signal inputs
5	R/W	Read/Write Pin	
6	E	Enable Pin	
7	DB_0	Code I/O Data LSB	• Data bus signals • DB_7 may also be used to check the busy flag • DB_0 to DB_3 are not used when interfacing with a 4-bit micoprocessor
8	DB_1	Code I/O Data 2nd Bit	
9	DB_2	Code I/O Data 3rd Bit	
10	DB_3	Code I/O Data 4th Bit	
11	DB_4	Code I/O Data 5th Bit	
12	DB_5	Code I/O Data 6th Bit	
13	DB_6	Code I/O Data 7th Bit	
14	DB_7	Code I/O Data MSB	

RECOMMENDED CONNECTORS [1]

USABLE CONNECTOR	CORRESPONDING CONNECTOR	MANUFACTURER
W-P5014	W-F1914	Showa Musen Kogyo K.K.
5267-14A	5264-14	Molex
FCN-724P014-AU/S	FCN-723J014/1	Fujitsu
65507-114	6539-023	Berg

NOTE:

1. FCN-723J014/1 and 6539-023 are interchangable.

OPTICAL CHARACTERISTICS ($V_{DD} - V_O = 4.0$ V, $t_A = 25°C$)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT	NOTE
$\theta_2 - \theta_1$	Viewing Angle Range	$\phi = 0°$	$C_0 \geq 2.0$	30	–	–	degrees	1
θ_1		$\theta_1 < \theta_2$	$C_0 = 2.0$	–	–	15		
θ_2				40	–	–		
$\theta_2 - \theta_1$		$\phi = 45°$ 315°	$C_0 \geq 2.0$	30	–	–		
θ_1		$\theta_1 < \theta_2$	$C_0 = 2.0$	–	–	20		
θ_2				45	–	–		
C_0	Contrast Ratio	$\theta = 15°$		2.0	3.0	–	–	2
t_R	Response Speed – Rise	$\theta = 15°$		–	150	300	ms	3
t_D	Response Speed – Decay	$\theta = 15°$		–	200	400	ms	

NOTES:

1. The viewing angle range is defined as shown in Figure 3.
2. Contrast ratio is defined as follows:
   When input signal is applied to the unit to select (turn on) the LCD dots (pixels) to be measured in the optical characteristics test method as defined in Figure 4:

$$\text{Contrast ratio} = \frac{\text{Photo–detector output voltage with non–select waveform being applied}}{\text{Photo–detector output voltage with select waveform being applied}}$$

3. When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Figure 4. The response characteristics of the photo-detector output are measured as shown in Figure 5.

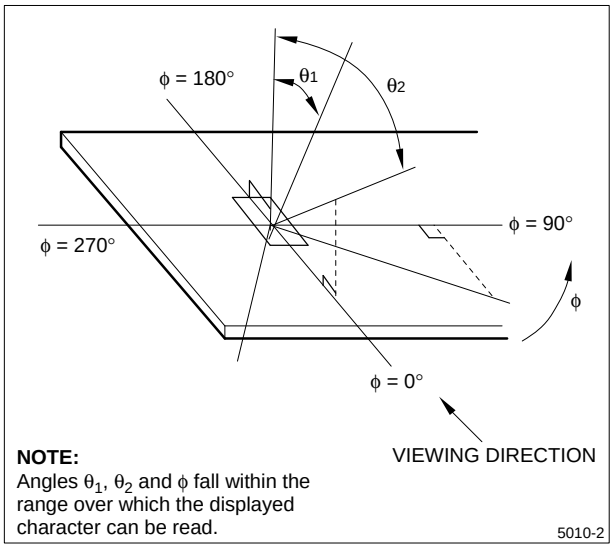


Figure 3. Definition of Viewing Angle

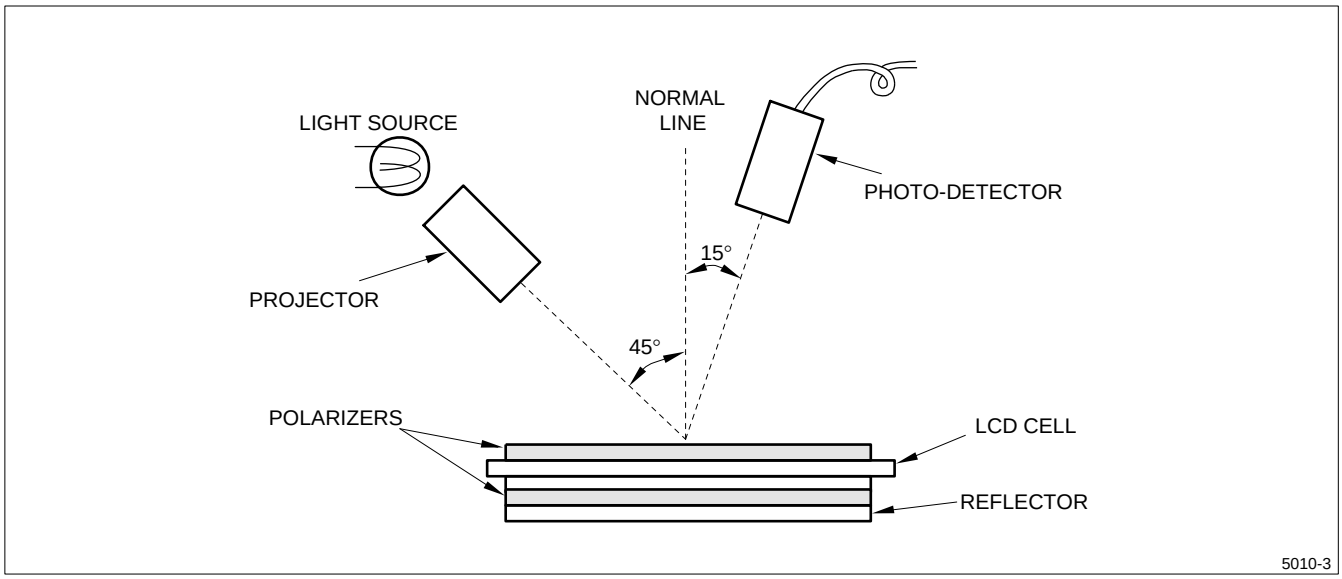


Figure 4. Optical Characteristics Test Method I

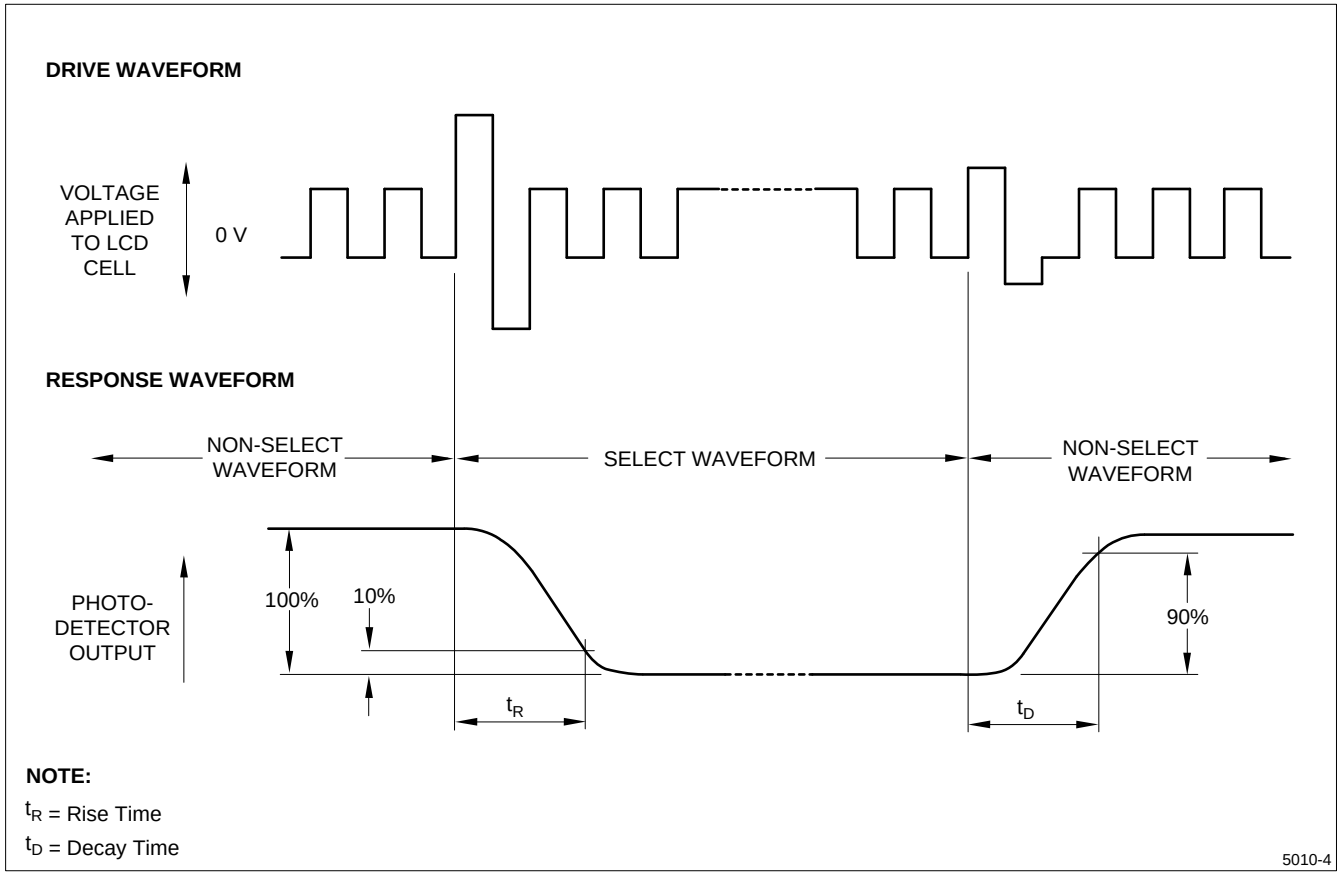


Figure 5. Definition of Response Time

PIN DESCRIPTION

V_{DD} and V_{SS} Pins

V_{DD} and V_{SS} pins are for power supply. V_{SS} pin is grounded, and V_{DD} pin is supplied with +5 V. The voltage necessary to drive the LCD is generated in the unit.

RS Pin

The controller LSI contains two 8-bit registers: instructions register (IR) and data register (DR).

RS pin selects these registers. IR serves to store instruction codes for display clear, shift, etc. and address information for display data RAM (DD RAM), character generator RAM (CG RAM); DR serves to temporarily store data to be written into DD RAM and CG RAM.

'0': Instruction register (Write)
Busy flag register; address counter (Read)

'1': Data register (Read/Write)

R/W Pin

Read or write selection signal pin.

'0': Write

'1': Read

E Pin

Data read or write operation enable signal pin.

DB_0 to DB_7 Pins

Tri-state bidirectional data bus pins. The bus allows data to be transmitted to or received from the external circuit. DB_7 serves also as busy flag output. When the unit is interfaced to a microcomputer with 4-bit parallel outputs, DB_0 to DB_3 pins are not used.

V_0 Pin

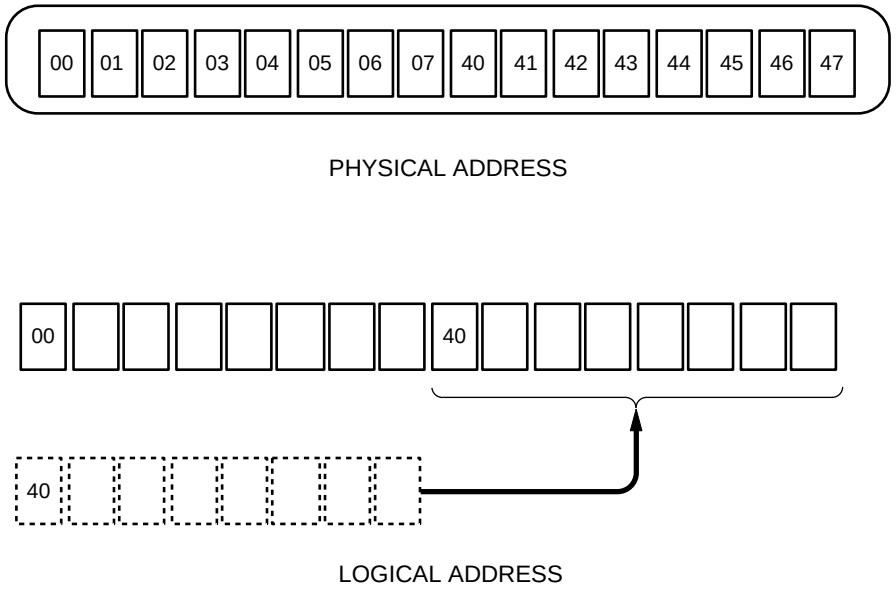
Viewing angle is varied and contrast is adjusted by changing input voltage between +5 V to 0 V by applying bias voltage to the LCD driver.

INSTRUCTION SET

INSTRUCTION	CODES										DESCRIPTION
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Display Clear	0	0	0	0	0	0	0	0	0	1	After entirely clearing the display, moves cursor to home position (address 0).
Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position (address 0). Restores display from shift. The contents of DD RAM remains unchanged.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Decides which direction cursor is to be moved and whether display is to be shifted. The above operaion is performed during a write or read cycle.
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Turns on and off display (D); cursor (C); blinks the character in the cursor position (B).
Cursor/ Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shifts the internal cursor and display while the contents of DD RAM remain unchanged.
Function Set	0	0	0	0	1	DL	1	0	*	*	Sets interface data length (DL).
CG RAM Address Set	0	0	0	1	A_{CG}						Sets CG RAM address (A_{CG}). The subsequent data is CG RAM data.
DD RAM Address Set	0	0	1	A_{DD}							Sets DD RAM address (A_{DD}). The subsequent data is DD RAM data.
Busy Flag/ Address Read	0	1	BF	A_C							Reads out busy flag (BF) denoting internal operation and address counter (AC).
CG RAM/ DD RAM Data Write	1	0	Write data								Writes data into DD RAM or CG RAM.
CG RAM/ DD RAM Data Read	1	1	Read data								Read data from DD RAM or CG RAM.

NOTES:

I/D = 1: Increment
S = 1: Display shift
D = 1: Display ON
C = 1: Cursor ON
B = 1: Character at cursor position blinks
I/D = 0: Decrement
S = 0: Display freeze
D = 0: Display OFF
C = 0: Cursor OFF
B = 0: Character at cursor position unblinks
S/C = 1: Display shift
R/L = 1: Right shift
DL = 1: 8 bits
BF = 1: During internal operation
S/C = 0: Internal cursor shift
R/L = 0: Left shift
DL = 0: 4 bits
BF = 0: End of internal operation



NOTE:
The display address is as above when the display is not shifted.
The second line's eight characters in logic correspond to the first line's right half eight characters in display because this unit is driven by 1/16 duty.

5010-6

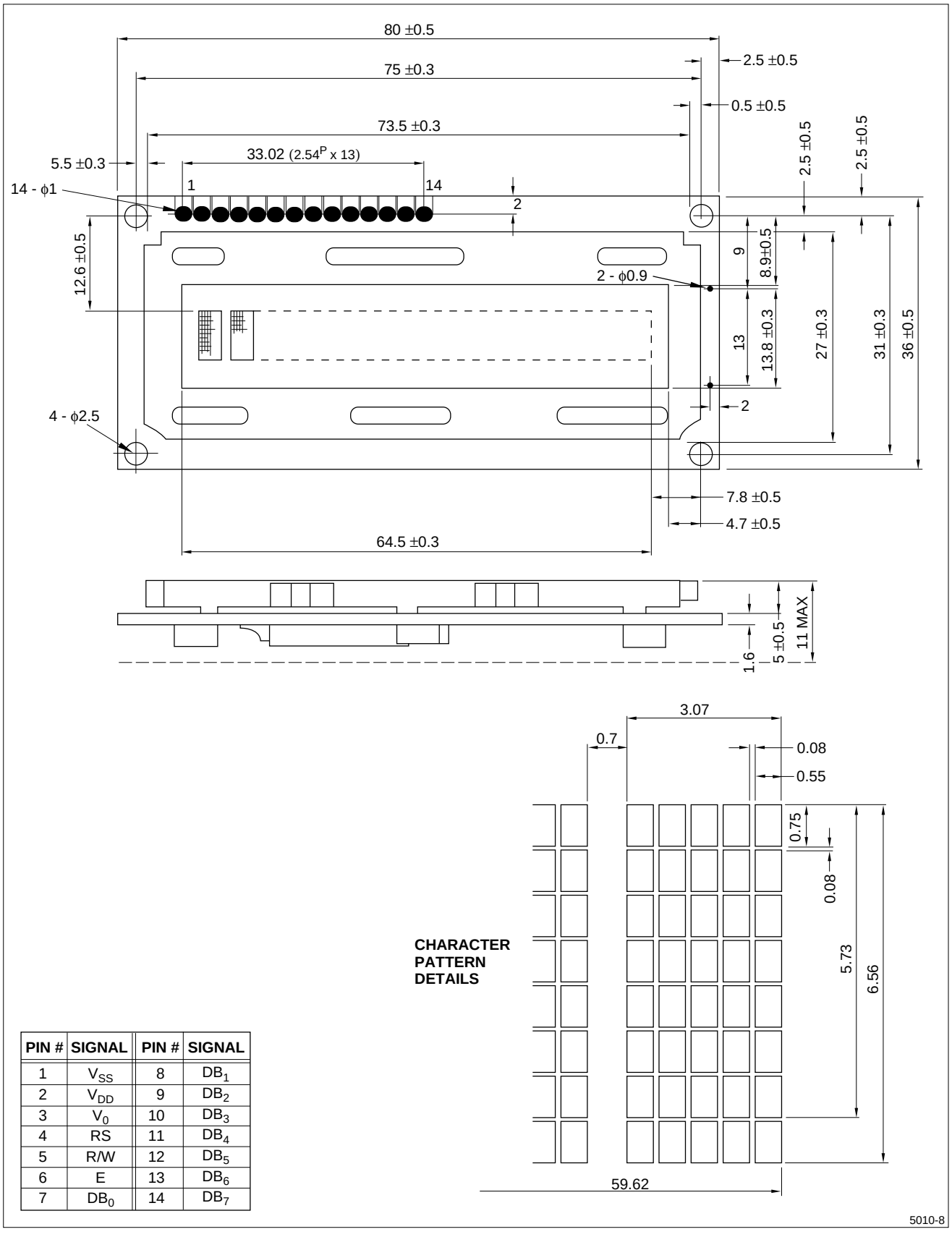
Figure 6. Display Address

HIGH-ORDER 4 BIT / LOW-ORDER 4 BIT	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxx0101	(6)												
xxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

NOTE: CG RAM is character generator RAM in which user-definable character patterns are stored.

Figure 7. Input Code Vs. Character Pattern

OUTLINE DIMENSIONS



PIN #	SIGNAL	PIN #	SIGNAL
1	V_{SS}	8	DB_1
2	V_{DD}	9	DB_2
3	V_0	10	DB_3
4	RS	11	DB_4
5	R/W	12	DB_5
6	E	13	DB_6
7	DB_0	14	DB_7